

MEMORY-BASED FINITE STATE MACHINE

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ABSTRACT

A programmable logic device is programmed to implement a finite state machine that may sequence through a plurality of states in a single clock cycle of the programmable logic device. The programmable logic device includes a plurality of programmable blocks programmed to instantiate memories. Each memory is programmed to determine a next state of the finite state machine based upon a current state of the finite state machine and current input conditions for the finite state machine.

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